What is claimed is:

1. A microcomputer comprising:

a first memory where a normal-operation program is stored;

a second memory where a functional test program stored;

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated;

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated;

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and

a test circuit which gives a preset specific instruction to said CPU when, in said test mode, a security test signal has been output from said CPU and a specific memory area has been accessed.

2. The microcomputer according to claim 1, wherein said specific instruction given to said CPU from said test circuit is a instruction which is to be detected by said

memory management unit as an illegitimate access.

3. A microcomputer comprising:

a first memory where a normal-operation program is stored;

a second memory where a functional test program stored;

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated;

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated;

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; and

an exception processing circuit, included in said CPU, for executing a predetermined exception process when said functional test program is executing a security test and said memory management unit has instructed execution of said specific operation.

4. A test method for a microcomputer having a memory

for storing a program, a central processing unit (CPU) which runs said program stored in said memory and a memory management unit which monitors an access to said memory and outputs an interrupt signal to said CPU upon detection of an illegitimate access, said test method sequentially executing:

a process of writing a jump instruction to jump to a second address in a first address in said memory;

a process of setting access to said second address as an illegitimate access in said memory management unit;

a process of jumping to said first address; and

a process of determining if there is a failure depending on whether or not said memory management unit has output said interrupt signal as a result of executing said jump instruction written at said first address.